LOW POWER COMPARATOR WITH FAST PROPAGATION DELAY

ABSTRACT OF THE DISCLOSURE

In at least a fast comparator configuration, the bias current applied to a current source within a comparator's input gain stage driven by a current proportional to the transconductance of a differential pair of input transistors receiving voltage signals to be compared is pulsed rather than continuous. The pulse with of the bias current is small relative to the system clock, but has a large current magnitude allowing the comparator to quickly respond to applied voltages, but without unacceptable increase in current and power consumption. A voltage limiter and hysteresis circuit minimize spurious currents when the bias current pulse is inactive. The bias current pulse and sampling of the comparator occur in predefined relation to the system clock.